We Claim:

1. A transistor array, comprising:

vertical FET transistors each formed of vertical and laterally parallel sections of active webs of semiconductor formed into a depth of a substrate;

said vertical FET transistors having a channel region surrounded by gate strips, forming a gate electrode and running along said sections of active webs, and forming word lines for a memory cell array of semiconductor memory cells assigned to the transistor array;

word line contacts electrically connecting at least some of said word lines to metal tracks of a metal plane superimposed on the transistor array;

an insulation in a deep trench, passing into the depth of said active web, insulating said word line contacts from other elements, the deep trenches being formed with a substantially identical structure as deep trenches otherwise forming storage capacitors in the memory cell array, except for a buried strap connecting said active web in the memory cell array to polysilicon in the depth of the substrate and that is omitted in the deep trenches of the word line contacts.

2. The transistor array according to claim 1, wherein the deep trench is filled with insulating material below said word line contact.

3. The transistor array according to claim 1, wherein said FET transistors are n-channel transistors, a thickness of said webs forming the semiconductor regions is 0.5 - 1 F, a length of each section of said webs forming an FET transistor is 2 - 3 F, a thickness of said word lines is approximately 0.2 F, and a vertical depth is approximately 5 F, where F is approximately equal to 70 nm.

4. The transistor array according to claim 3, wherein the conduction type of the first and second semiconductor wells is a p type.

5. A transistor array formed together with a memory cell array of semiconductor memory cells in a common first semiconductor well of a first conduction type in a substrate, the transistor array comprising:

vertical FET transistors each formed of vertical and laterally parallel sections of active webs of semiconductor formed into a depth of a substrate;

said vertical FET transistors having a channel region surrounded by gate strips, forming a gate electrode and running along said sections of active webs, and forming word lines for the memory cell array of semiconductor memory cells formed in the common well and assigned to the transistor array;

word line contacts electrically connecting at least some of said word lines to metal tracks of a metal plane superimposed on the transistor array;

all of said word lines leading into a second semiconductor well, separate and insulated from the first semiconductor well and having the same conduction type, and said word line contacts connecting said word lines to the metal tracks of the metal plane in the second semiconductor well.

6. The transistor array according to claim 5, wherein:

said active webs inside the second semiconductor well, supporting said word lines on both sides thereof, are insulated from corresponding said web sections outside the second semiconductor well by insulating columns inside deep trenches passing through said webs at an interface between the second semiconductor well and a surrounding semiconductor region of a second conduction type;

said deep trenches being formed with a substantially identical structure as deep trenches otherwise forming storage capacitors in the memory cell array, except of a buried strap connecting an active web in the memory cell array to polysilicon lying in a depth of the substrate and being omitted in the deep trenches at the interface between the second semiconductor well and the surrounding semiconductor region.

7. The transistor array according to claim 5, wherein said FET transistors are n-channel transistors, a thickness of said webs forming the semiconductor regions is 0.5 - 1 F, a length of each section of said webs forming an FET transistor is 2 - 3 F, a thickness of said word lines is approximately 0.2 F, and a vertical depth is approximately 5 F, where F is approximately equal to 70 nm.

8. The transistor array according to claim 5, wherein the conduction type of the first and second semiconductor wells is a p type.

9. A semiconductor memory configuration, comprising a transistor array of FET transistors according to claim 1 wherein each memory cell of the memory cell array is assigned one vertical FET transistor.

10. The memory configuration according to claim 9 formed as a DRAM memory.

11. A semiconductor memory configuration, comprising a transistor array of FET transistors according to claim 5 wherein each memory cell of the memory cell array is assigned one vertical FET transistor.

12. The memory configuration according to claim 11 formed as a DRAM memory.